

FORM PTO-1449			U.S. Department of Commerce Patent and Trademark Office		Atty. Docket No. FIS920030232US1		Application No. 10/707,996	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)			Applicant Daniel C. EDELSTEIN et al.					
			Filing Date 01/30/2004		Group 2813			
U.S. PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
<i>[Redacted]</i>								
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
<i>Rhr</i>		V. Arnal, et al., "A Novel SiO ₂ Air Gap Low K for Copper Dual Damascene Interconnect." Conference Proceedings of the Advanced Metallization Conference 2000, pp. 71-76						
		A. P. Li, et al., "Hexagonal Pore Arrays with a 50-420 nm Interpore Distance Formed by Self-Organization in Anodic Alumina." Journal of Applied Physics, vol. 84, no. 11, December 1, 1998, pp. 6023-6026						
		O. Jessensky, et al., "Self-Organization Formation of Hexagonal Pore Arrays in Anodic Alumina." Journal of Applied Physics, vol. 72, no. 10, March 9, 1998, pp. 1173-1175.						
		A. P. Li, et al., "Polycrystalline Nanopore Arrays with Hexagonal Ordering on Aluminum." Journal of Vacuum Science and Technology, vol. 17, no. 4, July/August 1999, pp. 1428-1431.						
		L.G. Gosset, et al., "General Review of Issues and Perspectives for Advanced Copper Interconnections Using Advanced Copper Interconnections Using Air Gaps as Ultra-Low K Material." IEEE 2003, pp. 65-67.						
		V. Arnal, et al., "Integration of a 3 Level Cu - SiO ₂ Air Gap Interconnect for Sub 0.1 micron CMOS Technologies." IEEE 2001, pp. 298-300.						
<i>✓</i>		C.T. Black, et al., "Integration of Self-Assembled Diblock Copolymers for Semiconductor Capacitor Fabrication." Applied Physics Letters, vol. 79, no. 3, July 16, 2001, pp.409-411						
<i>Rhr</i>		Z. Liu, et al., "Metal Nanocrystal Memories – Part I: Device Design and Fabrication." IEEE Transactions on Electron Devices, vol. 49, no. 9, September 2002, pp.1606-1613.						
EXAMINER	<i>hasee Schley</i>			DATE CONSIDERED		<i>12/25/06</i>		
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								